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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,537	03/11/2004	Rajesh S. Nair	ONS00507	4381

7590 07/11/2005

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EXAMINER	
ROSE, KIESHA L	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,537	NAIR ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the filing of the application.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Fig. 1, #'s 14 and 49

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tihanyi (U.S. Patent 6,507,071).

Tihanyi discloses a high voltage transistor (Figs. 2 and 3) that contains a semiconductor substrate (1) having a first conductivity type (N), a region of semiconductor material (2) comprising alternating layers of first and second conductivity type material over the substrate having a major surface, a drain region (9) of the second conductivity type (P) extending from the first major surface into at least a portion of the region semiconductor material, a body region (11) of the first conductivity type formed in a portion of the region of semiconductor material and extending partially from the first major surface into the region of semiconductor material, a first source region (10) formed in the body region and a trench gate structure (14) formed in a portion of the region of semiconductor material and controls a sub-surface channel region, the drain region comprises a trench filled with doped polycrystalline material and trench gate structure is filled with doped polycrystalline material of second conductivity type and extends from the first major surface adjacent the source region and a portion of the body region into the region of semiconductor material and includes a gate dielectric layer (12) formed at least on a sidewall surface of the trench gate structure, where a surface gate structure (gate over the trench) is formed over the major surface, a lower portion of the trench gate structure terminates within the substrate, a one layer of alternating layers adjacent the first major surface comprises a first conductivity type and

is thicker than adjacent layers of semiconductor material and a doped region (one of the alternating layers) adjacent the first major surface and between the body and drain region.

Claims 10,11 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tihanyi.

Tihanyi discloses a high voltage transistor (Figs. 2 and 3) that contains a semiconductor substrate (1), a region of semiconductor material (2) including a plurality of alternating layers of first and second conductivity semiconductor material formed over the semiconductor substrate and having a major surface, a trench drain structure (9) formed in the region of semiconductor material, a trench gate structure (14) formed in the region of semiconductor material, a body region (11) of first conductivity type formed adjacent the trench gate structure, a source region (10) of second conductivity type formed in the region of first conductivity type, a surface gate portion (gate that extends over the major surface) formed over the major surface adjacent the trench gate structure and source region, the region of semiconductor material includes a layer of first conductivity type at major surface that is thicker than the adjacent layers of the region of semiconductor material, a portion of the alternating layers extend between the trench drain and trench gate and the trench drain is filled with a polycrystalline material of second conductivity type.

Claims 17,18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tihanyi.

Tihanyi discloses a high voltage transistor (Figs. 2 and 3) that contains alternating layers (2) of first and second conductivity type material forming a semiconductor region, a trench gate structure (14) formed in the alternating layers and controls a sub-surface channel region, a drain region (9) of second conductivity spaced apart from the trench gate and extending into the alternating layers, a source region (10) of second conductivity type formed adjacent to the trench gate and the drain region is filled with polycrystalline semiconductor material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tihanyi in view of Disney (U.S. Patent 6,509,220).

Tihanyi discloses all the limitations except for a first doped region of second conductivity type adjacent a portion of the sidewall of the trench gate structure. Whereas Disney discloses a high voltage transistor (Figs. 4 and 5) that contain a trench gate structure (63) with a gate dielectric layer (62) along the sidewall with a first doped region (41) of second conductivity type (P) formed adjacent the sidewall. The doped region is formed to increase the integrity of the source-to-substrate connection and reduce susceptibility of the device to parasitic bipolar effects. (Column 7,lines 8-11)

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tihanyi by incorporating a first doped region to increase the integrity of the source-to-substrate connection and reduce susceptibility of the device to parasitic bipolar effects as taught by Disney.

Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tihanyi in view of Disney (U.S. Patent 6,509,220).

Tihanyi discloses all the limitations except for a first doped region of second conductivity type adjacent a portion of the sidewall of the trench gate structure and trench gate structure extend further than the trench drain structure. Whereas Disney discloses a high voltage transistor (Figs. 4-6) that contain a trench gate structure (63) that extends into the substrate with a gate dielectric layer (62) along the sidewall with a first doped region (41) of second conductivity type (P) formed adjacent the sidewall and a trench drain structure (67) formed at a depth less than the depth of the trench gate structure. The doped region is formed to increase the integrity of the source-to-substrate connection and reduce susceptibility of the device to parasitic bipolar effects. (Column 7,lines 8-11) This configuration is formed with the trench gate being deeper than the trench drain to provide a low on-state resistance for a given breakdown voltage. (Column 4, lines 1-4) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tihanyi by incorporating a first doped region to increase the integrity of the source-to-substrate connection and reduce susceptibility of the device to parasitic bipolar effects

and the trench gate to be deeper then the trench drain to provide a low on-state resistance for a given breakdown voltage as taught by Disney.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tihanyi in view of Disney (U.S. Patent 6,509,220).

Tihanyi discloses all the limitations except for the trench gate structure to extend deeper than the drain region. Whereas Disney discloses a high voltage transistor (Figs. 4 and 5) that contain a trench gate structure (63) that extends to the substrate and a drain region (67) which does not extend as deep as the trench gate structure. This configuration is formed with the trench gate being deeper than the trench drain to provide a low on-state resistance for a given breakdown voltage. (Column 4, lines 1-4) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Tihanyi by incorporating the trench gate to be deeper then the trench drain to provide a low on-state resistance for a given breakdown voltage as taught by Disney.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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ARIAN ZARABIAN
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